REMARKS

In the Office Action, Examiner rejected Claims 1, 4 and 8 under 35 U.S.C. 103(a) as being obvious over Chang et al. (U.S. Patent No. 6,218,726) in view of Moberly (U.S. Patent No. 6,484,280). Further, Examiner rejected Claims 3, 6 and 7 under 35 U.S.C. 103(a) as being obvious over Chang et al. The examiner stated that Claims 2, 5 and 9 are objected to because of the informalities but would be allowable if the informalities are corrected and rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Accordingly, the applicant has amended the set of claims to more clearly differentiate the present invention from the technologies disclosed by the cited references. In the amendment, the limitations in Claim 2 have been included in Claim 1, the limitations in Claim 5 have been included in Claim 4, and the limitations in Claim 9 have been included in Claim 8, respectively. Claims 2, 5 and 9 have been canceled.

The technology disclosed by the cited Chang et al. reference is different from the present application in the following respects. The cited Chang reference describes a method to determine thermo-mechanical stress or shear stress between two metal layers. IC fabrication process contains various chemical and thermal processes; because of the difference in thermal expansion of two materials, silicon wafer is subjected to thermo-mechanical stresses. In IC fabrication, multiple layers are deposited on top

of each other; it is necessary to know the thermo-mechanical stress between two layers to avoid deformities. The cited Chang et al. reference describes that diagonally positioned linear metal trace on top of L shaped metal trace can be used to determine thermo-mechanical stress between two layers. With change in temperature, the resistivity of each metal and the resistivity of dielectric separating the metal changes; thus, the leakage current from one layer to another layer changes. The cited Chang el al. reference explains that by measuring the change in leakage current in this special structure (diagonal metal trace over L shaped trace), one can determine the amount of thermo-mechanical stress between two layers.

It should be noted that the objective and procedure described in the cited Chang el al. reference is different from the present application. In the cited Chang et al. reference, the two metal layers are kept separated by an insulating material layer in-between (isolation layer 40), and no electrically conductive connection is made between the two metal layers (see Figure 4). In contrast, the basic principle in the present invention is to make connections through various metal layers using via holes as shown in Figures 4A and 4B. It does not measure leakage current unlike the process disclosed by the cited Chang et al. reference. Nevertheless, to more clearly distinguish the present invention, the applicant has amended Claims 1 to include the limitations of

Claim 2. Similarly, the applicant has amended Claims 4 and 8 to include the limitations of Claims 5 and 9, respectively.

The cited Moberly reference (US patent number 6,484,280) is essentially the IEEE P1500 design, which has the following characteristics: (1) the design of each block is modified by surrounding it by flip-flops (called as wrapper); (2) these flip-flops are designed to operate in special mode as shift register (figure 3); (3) the mode of operation is controlled by a number of control signals and a finite state machine (IEEE Test Access Port, TAP); (4) Data is scan-in (by TDI pin) or scan-out (by TDO pin); (5) internal nodes are not directly observable nor probed, the logic value is inferred through the data obtained through scan-out operation (TDO pin).

As mentioned above, this is essentially IEEE P1500 design and it is disclosed in the present application as prior art (Figure 2A); one can compare Fig. 2A in the present application with Fig. 4 in the cited Moberly reference. Further, the present application also disclosed a couple of example designs of wrapper cells as prior art (Fig. 2B and 2C), where flip-flops designed with multiplexers support scan-in/scan-out operation. It is also worth mentioning that few other comparable methods exists as described in the background section of the present application.

In contrast, the basic concept in the present invention is to connect internal nodes of the integrated circuit (IC) to the top-level metal layer. In the present day IC fabrication technology,

it is possible through successive connections to the upper level layers using via holes. This concept is illustrated in Figures 4A and 4B of the present application. As top-level metal layer is on the surface of the IC, such connection effectively brings up these internal nodes to the surface of the IC. The surface of an IC can be readily probed for testing through existing contact probes. Thus, by probing these extensions, one can effectively probe internal nodes through the top-level metal layer. It should be noted that without such extension, internal nodes are buried and hence, cannot be probed. Further, in this method of the present invention, there is no change in the design of any circuit element such as flip-flops, instead there is a change in metal mask used in the fabrication process. The applicant believes that there is no notion of such concept in any of the cited references, individually or in combination thereof.

As described in the background section of the present application, because internal nodes cannot be probed at the present time, various design-for-testability (DFT) methods are used to determine the logic state of internal nodes. Scan design, boundary scan design, IEEE P1500 design are few examples of such DFT methods. In all these methods, the design of flip-flops is modified; in a special mode, flip-flops behave as shift register; by shifting bits, one can determine the logic state that was captured in the flip-flop. It should be noted that only scan-in and scan-out points are directly observable; in other words, at-

most there are two nodes that can be probed (scan-in and scan-out). The logic states for all other internal nodes are inferred through the data obtained at scan-out point. In contrast, in the present invention, there is no modification of any circuit elements (i.e. flip-flops), no scan-in/scan-out operation and all internal nodes become the probe points.

In this opportunity, the applicant has amended the specification to correct the minor errors therein and to more clearly disclose the present invention. This is to verify that no new matter has been introduced by this amendment.

Further in this opportunity, the applicant has amended the drawings to add a "Prior Art" label to Figures 1, 2A-2C and 4A. Replacement sheets for the amended drawing are also submitted.

In view of the foregoing, Applicant believes that Claims 1, 3-4, 6-8 are in condition for allowance, and accordingly, Applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

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Dated: 3/15/05

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